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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,031	07/14/2003	James D. Pylant	067810/0303880 PI-018	1179

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EXAMINER	
HUYNH, LOUIS K	
ART UNIT	**PAPER NUMBER**
3721	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,031	PYLANT ET AL.	
	Examiner	Art Unit	
	Louis K. Huynh	3721	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's cancellation of claims 1-14 in paper filed on April 18, 2005 is acknowledged.

2. Claims 15-18 and new claims 19-22 are pending in the present application.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 15-18 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15, lines 3-4: "placing each wafer on a corresponding wafer frame to obtain a plurality of wafer assemblies" is ambiguous and indefinite because each wafer and its corresponding wafer frame can only form a single wafer assembly; therefore, in order to obtain a plurality of wafer assemblies, the step of placing must be repeated at least twice. Applicant is respectfully requested to amend the claim to clearly recite the proper steps leading to obtaining a plurality of wafer assemblies.

Claim 15, line 10: "each wafer element" lacks proper antecedent basic.

Claim 22, line 3: "wafer frame" lacks proper antecedent basic.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 15-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawada (US 6,119,865) in view of Takeuchi et al. (5,238,876).

With respect to Claims 1-18, Kawada discloses a method of storing a plurality of wafer assemblies including the steps of: placing a wafer (4) on an adhesive sheet (3), adhering the adhesive sheet (3) to a frame (2) to form a wafer assembly (1) (col. 2, lines 17-30), sequentially placing and aligning each of a plurality of wafer assemblies (1) into a container (15) along orientation artifacts (16) disposed inside of the container (15) in order to form a stack of wafer assemblies, and covering the container with a cover (17). The method of Kawada meets all of applicant's claimed subject matter but lacks the specific teaching of the wafer frame having at least one alignment artifact disposed thereon for aligning with the orientation artifacts disposed inside the container in order to prevent substantial rotational movement of the wafer assembly within the container.

However, it is known in the art that a wafer frame is not always in a perfect circular shape as disclosed in the exemplary embodiment of Kawada. For example, Takeuchi discloses a wafer assembly including a ring frame (11), a wafer (1), a tape (10) for holding the wafer (1) to the frame (11); wherein the ring frame (11) has alignment artifacts (straight edges) along the perimeter for mounting onto a chuck (12) in a dicing process such that the alignment artifacts prevent the wafer from rotational movement while the wafer being divided.

Therefore, it would have been obvious to an ordinary skilled person in the art, at the time the invention was made, to have modified the method of Kawada by having replaced the circular wafer frame with one having alignment artifacts, such as one disclosed by Takeuchi, since wafer

frame with such alignment artifacts are known for providing alignment in wafer and IC chips manufacturing processes.

Note that care must be taken when handling wafer assemblies because the orientation of the wafer assemblies must be known at all times during processing and/or storage; therefore, the wafer assemblies of Takeuchi should have the same orientation when being placed into the container of Kawada, and the orientation of the wafer assemblies of Takeuchi can be recognized by the notches on one of the sides of the wafer frame as depicted in FIG. 2A of the Takeuchi reference. Thus, placing the wafer assemblies such that visualization of such orientation marks when the container is uncovered would have been an obvious matter to the skilled person in the art. Moreover, the alignment artifacts (straight edges) of the wafer frame of Takeuchi would align with the orientation artifacts (16) of the container (15) of Kawada and would prevent substantial rotational movement of the wafer assembly within the container.

With respect to Claims 19 and 22, Kawada discloses a method of storing a plurality of wafer elements including the steps of: providing a plurality of wafer element (1) comprising a wafer (4), an adhesive sheet (3) and a frame (2); placing and aligning each of a plurality of wafer elements (1) into a container (15) along orientation artifacts (16) disposed inside of the container (15) in order to form a stack of wafer assemblies. The method of Kawada meets all of applicant's claimed subject matter but lacks the specific teaching of the wafer element having at least one alignment artifact disposed thereon for engaging and aligning with the orientation artifacts disposed inside the container.

However, it is known in the art that a wafer frame is not always in a perfect circular shape as disclosed in the exemplary embodiment of Kawada. For example, Takeuchi discloses a wafer element including a ring frame (11), a wafer (1), a tape (10) for holding the wafer (1) to the frame (11); wherein the ring frame (11) has alignment artifacts (straight edges) along the perimeter for mounting onto a chuck (12) in a dicing process such that the alignment artifacts prevent the wafer from rotational movement while the wafer being divided.

Therefore, it would have been obvious to an ordinary skilled person in the art, at the time the invention was made, to have modified the method of Kawada by having replaced the circular wafer frame with one having alignment artifacts, such as one disclosed by Takeuchi, since wafer frame with such alignment artifacts are known for providing alignment in wafer and IC chips manufacturing processes.

With respect to Claims 20 and 21, note that care must be taken when handling wafer elements because the orientation of the wafer elements must be known at all times during processing and/or storage; therefore, the wafer elements of Takeuchi should have the same orientation when being placed into the container of Kawada, and the orientation of the wafer elements of Takeuchi can be recognized by the notches on one of the sides of the wafer frame as depicted in FIG. 2A of the Takeuchi reference. Thus, placing the wafer elements such that visualization of such orientation marks when the container is uncovered would have been an obvious matter to the skilled person in the art.

Response to Arguments

7. Applicant's arguments filed April 18, 2005 have been fully considered but they are not persuasive.

8. Applicant contends that the slots (16) disposed in the Kawada reference (US 6,119,865) do not function to orient wafers assemblies (1) and they lack the contour that permits engagement with a wafer element, and that the orientation of the wafer assemblies are not visible when the container is uncovered. Applicant further contends that the reference to Takeuchi fails to remedy the deficiencies of Kawada because the ring frame (11) of Takeuchi is not constructed to mate with at least one locating portion of a framed wafer, and that Takeuchi fails to teach or suggest storing a stack of wafers in a manner that would allow the orientation of the stack to be visible and known.

9. This is not found persuasive because the reference to Kawada discloses a method of storing a plurality of wafer assemblies and the reference to Takeuchi discloses typical and practical wafer assemblies; and it is known in the art that a plurality of wafer assemblies are to be accommodated in a container during transfer between processing stations and/or storage. Therefore, at the time the invention was made, placing the wafer assemblies of Takeuchi into a container such as the container of Kawada for storage and/or transfer between processing stations would have been an obvious matter to a skilled person in the art.

10. In regard to the visibility of the orientation of the stack of wafers when the container is uncovered, it is well known in the art that care must be taken with respect to orientation when handling wafer assemblies because the orientation of the wafer assemblies must be known at all times during processing and/or storage; therefore, the wafer assemblies of Takeuchi should have

the same orientation when being placed into the container of Kawada, and the orientation of the wafer assemblies of Takeuchi can be recognized by the notches on one of the sides of the wafer frame as depicted in FIG. 2A of the Takeuchi reference. Thus, placing the wafer assemblies such that visualization of such orientation marks when the container is uncovered would have been an obvious matter to the skilled person in the art.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

12. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Louis K. Huynh whose telephone number is (571) 272-4462. The examiner can normally be reached on M-F from 9:30AM to 5:00PM.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rinaldi I. Rada can be reached on (571) 272-4467. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Louis K. Huynh
PRIMARY EXAMINER
Art Unit 3721

May 23, 2005